

Test Report V1.0
Single Event Effects (SEE) Testing of the Memtek Asynchronous
Electrically Erasable Programmable Read-Only Memory (EEPROM) 4096x16

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I. Introduction

The EEPROM 4096x16 is a non-volatile memory in a configuration of 4,096 words x 16 bits, which are accessed like static-RAM. The Memtek part uses a pseudo-SRAM interface similar to conventional asynchronous SRAM (it should be noted that some normally used pins have no electrical connection within the package), having a maximum read cycle frequency of 5 MHz. The write cycle is on the order of 10ms. The EEPROM utilizes the Fowler-Nordheim tunneling mechanism to move charge in and out of an electrode. The voltage needed to program and erase the memory is between 13V and 14V, which is internally generated by a charge pump.

II. Tested Devices

The Memtek devices were designed and fabricated by Memtek, LLC. All devices were characterized prior to exposure, both at NASA-GSFC facility and onsite prior to scheduled beam time. The two devices tested for single event effects (SEE) are from a total of four, two of which are reserved for total dose testing. Complete package markings for the devices are:

17302-001

Additional Part Information:

Device: EEPROM_X35_1
Device name: TC2_2_4
Device type: Asynchronous Non-Volatile Memory
Memory Organization: 4096 x 16
Technology Node: 0.35 Micron
Process Flow: C35E (0.35µm Embedded Flash Process)
Part Number: 17302_001
Run Number: B23266.L1
Wafer # 6
Package type: 68 pin ceramic leaded package (unsealed top)
Fabrication Date: Feb. 28, 2005

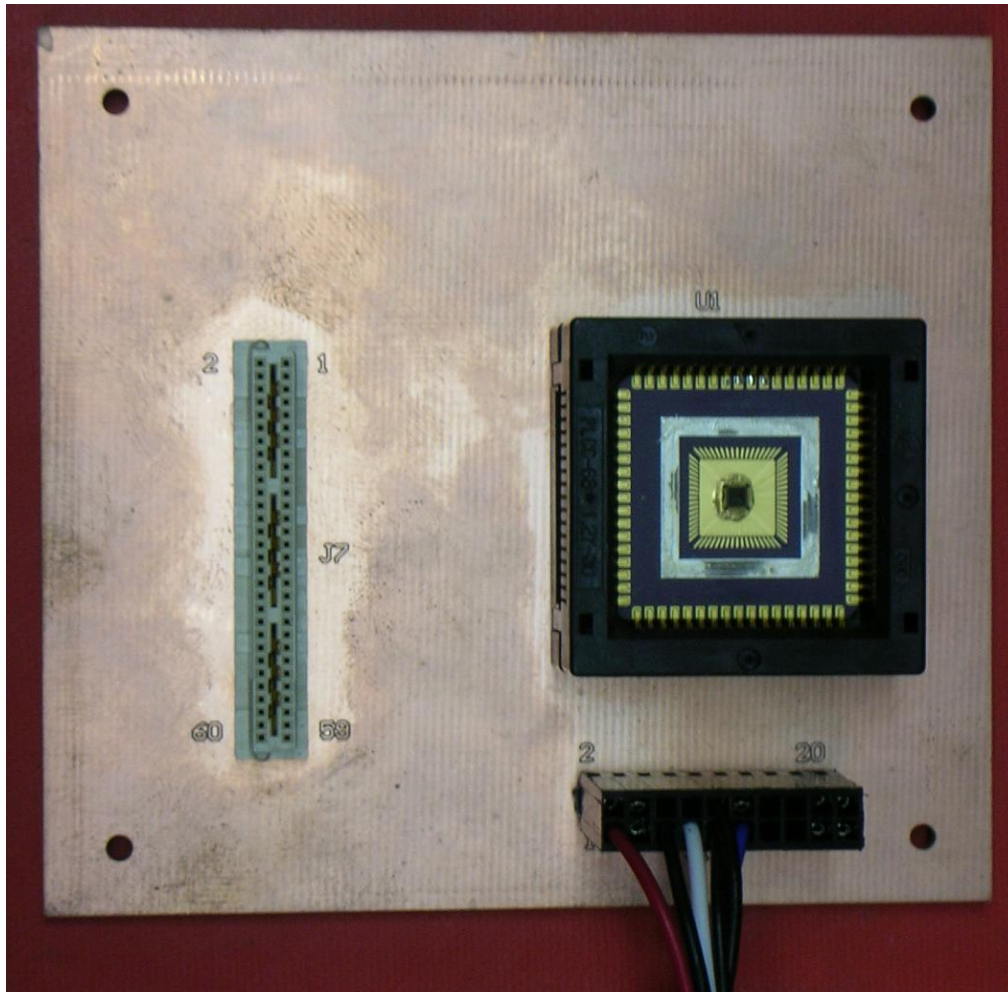


Figure 1: Delided part number 105 in daughter card socket

III. Test Facility

Facility: Texas A&M University Cyclotron Single Event Effects Test Facility using the 15 MeV/amu tune.

Beam Time: 8 hours

Flux Used: 1×10^4 to 1.3×10^5 p/cm²/s

Minimum Fluence Achieved per Part: 3.25×10^7 p/cm²

Ions used	LET (MeV.cm ² /mg)
Ar	8.6
Kr	29.1
Xe	53.5

Table 1: TAMU beam properties

IV. Test Methods

Temperature: room temperature (25 C)

Test Voltage: nominal (3.0 Volts)

Operating Frequency: 4.347 GHz

Test Hardware:

The Low Cost Digital Tester (LCDT) was used to perform this testing. A socket-held Device Under Test (DUT) on daughter card was developed and shown above in Figure 1. The appropriate VHDL was written to the LCDT in order to perform the required SEE testing as detailed below. Appropriate power supplies were used with the DUT, current strip charted, and monitored for over-current conditions during all tests.

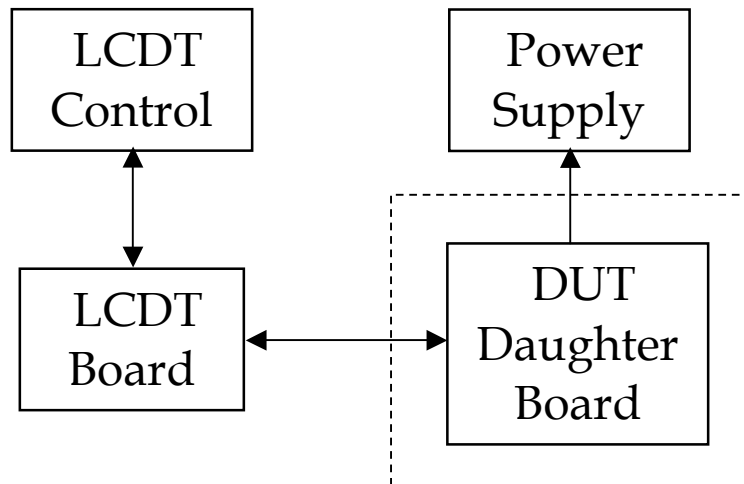


Figure 2: Block Diagram of test setup, where the dashed line represents the component within the ion beam path

Procedure:

Prior to exposure a test pattern was written to the memory cells. Then the test was run either statically or dynamically (read after beam exposure or continuously during beam exposure; respectively) until a desired fluence was met.

V. Test Results

Expected Single Event Errors (SEE):

Single Event Upset (SEU) – Single and/or multi-bit errors, as well as multi-cell errors when the memory is read. A known pattern is written and expected when read; any variation from the known pattern will show this type of SEE.

Single Event Functional Interrupt (SEFI) – Unexpected mode changes, test modes, halt, pointer errors, etc. This type of SEE can be observed if excessive errors occur and no longer remain after the part is power cycled and reset.

Single Event Latch-up (SEL) – Latch-up, an electrical condition, may occur if the internal resistance of a part's region allowing for over-current conditions to occur. This type of SEE can be seen in the supply current value exceeding the maximum current described in the part's datasheet.

Observed SEE:

SEUs: Single event upsets were shown to occur only in dynamic tests, and were recorded as errors that did not remain for multiple read cycles.

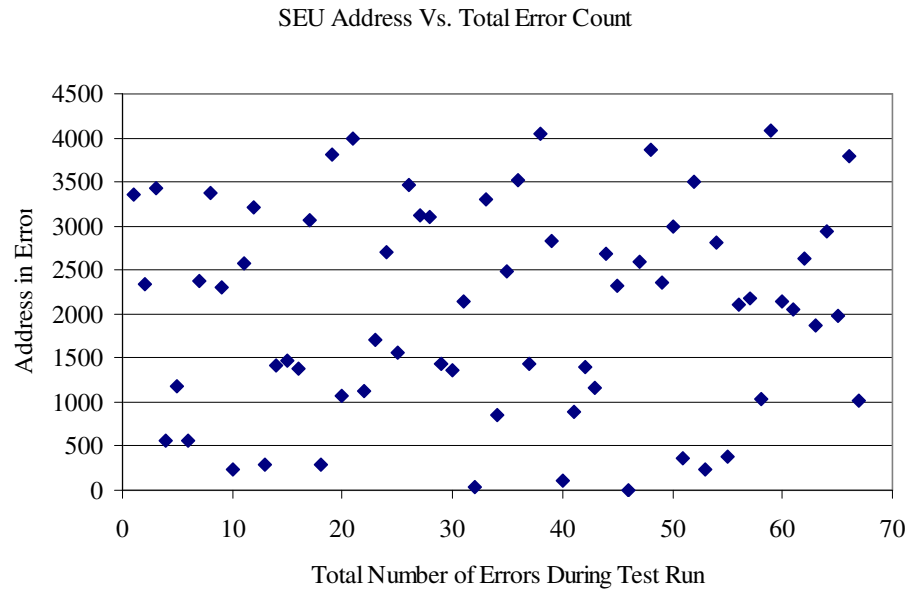


Figure 3: Single event upsets in varied addresses during a dynamic run.

In order to confirm that the physical locations of the upsets were not clustered together, the device layout was compared with address in error information. Figure 4 shows all errors in the memory space after one run.

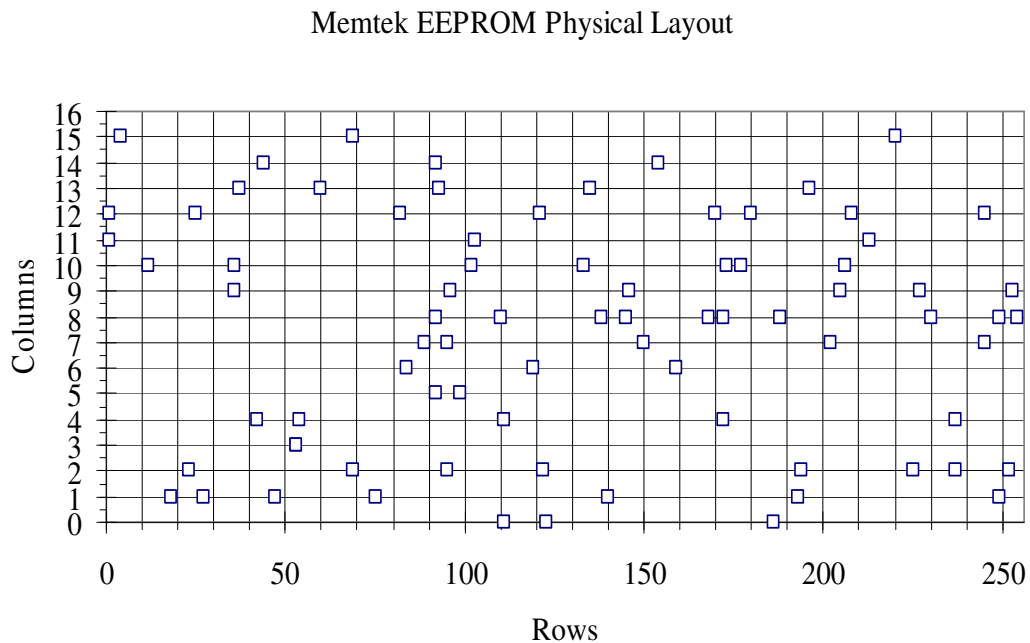


Figure 4: Errors recorded in the memory space of the device

SEFIs: Functional interrupts were found to occur only in dynamic runs, similar to the SEUs that were recorded. However, the functional interrupts were reflected in the data as continuous errors in all addresses in a repeating fashion. This result is most likely from an incident on circuitry external to the memory cells.



Figure 4: Functional interrupt shown after 150 errors were collected

SELs: Latching only occurred at an LET of 53.5 MeV.cm²/mg. Latch-up was observed on the current monitor for the device's power supply. A spike in the current automatically discontinued power supply to the device and is shown in the data as can be seen below.

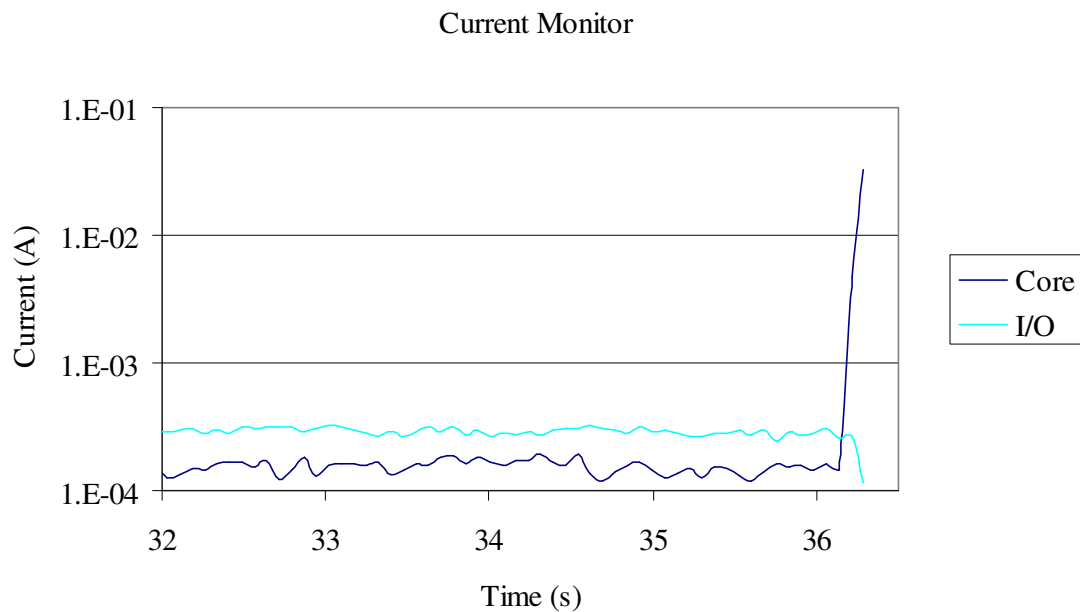


Figure 5: Over current occurrence during a static run.

Part Result Summary:

The EEPROM memory cells are susceptible to SEUs at various LET. However, the errors that occur have no stuck bits recorded up to 53.5 MeV.cm²/mg.

The more prevalent upset would be a functional interrupt. In the event of a functional interrupt the part would have to be power cycled to restore its function. However, these interrupts show results that point to the error occurring external to the memory cells.

There are no static upsets in the memory cells; however this does not mean that the cells are immune to radiation, there are latch-ups at the highest LET, and this could be occurring because of either the memory cells and/or the address circuitry. After mapping the physical layout, it was found that multi-bit upsets were not found to occur in subsequent error records on any runs. Latch-up occurrences limit the use of this part in hostile environments and could damage the parts although none failed after being power cycled. The test engineers precautions of over-current provided that this damage did not occur. To find the threshold for latch-up would require further testing, and is only recommended if intended for use in radiation environments.

Repairable errors: SEU, SEFI (with power cycle)

Non-repairable: SEL

Table 2 below summarizes what results occurred at the tested LETs. From this and the recorded fluence we can extract the device's cross section which is shown in Figure 6.

Part	Tests	LET (MeV.cm ² /mg)			Total Dose (krad)
		8.6	29.1	53.5	
Results For 105	static	No Errors Recorded	No Errors Recorded	2 SELs, 0 SEUs, 0 SEFIs	16.3
	dynamic	21 SEUs, 0 SEFIs, 0 SELs	230 SEUs, 2 SEFIs, 0 SELs	316 SEUs, 5 SEFIs, 4 SELs	
Results For 106	static	No Errors Recorded	No Errors Recorded	No Errors Recorded	20.1
	dynamic	14 SEUs, 0 SEFIs, 0 SELs	136 SEUs, 4 SEFIs, 0 SELs	807 SEUs, 8 SEFIs, 2 SELs	

Table 2: Part results at different LET values

Dynamic Address in Error Cross Section

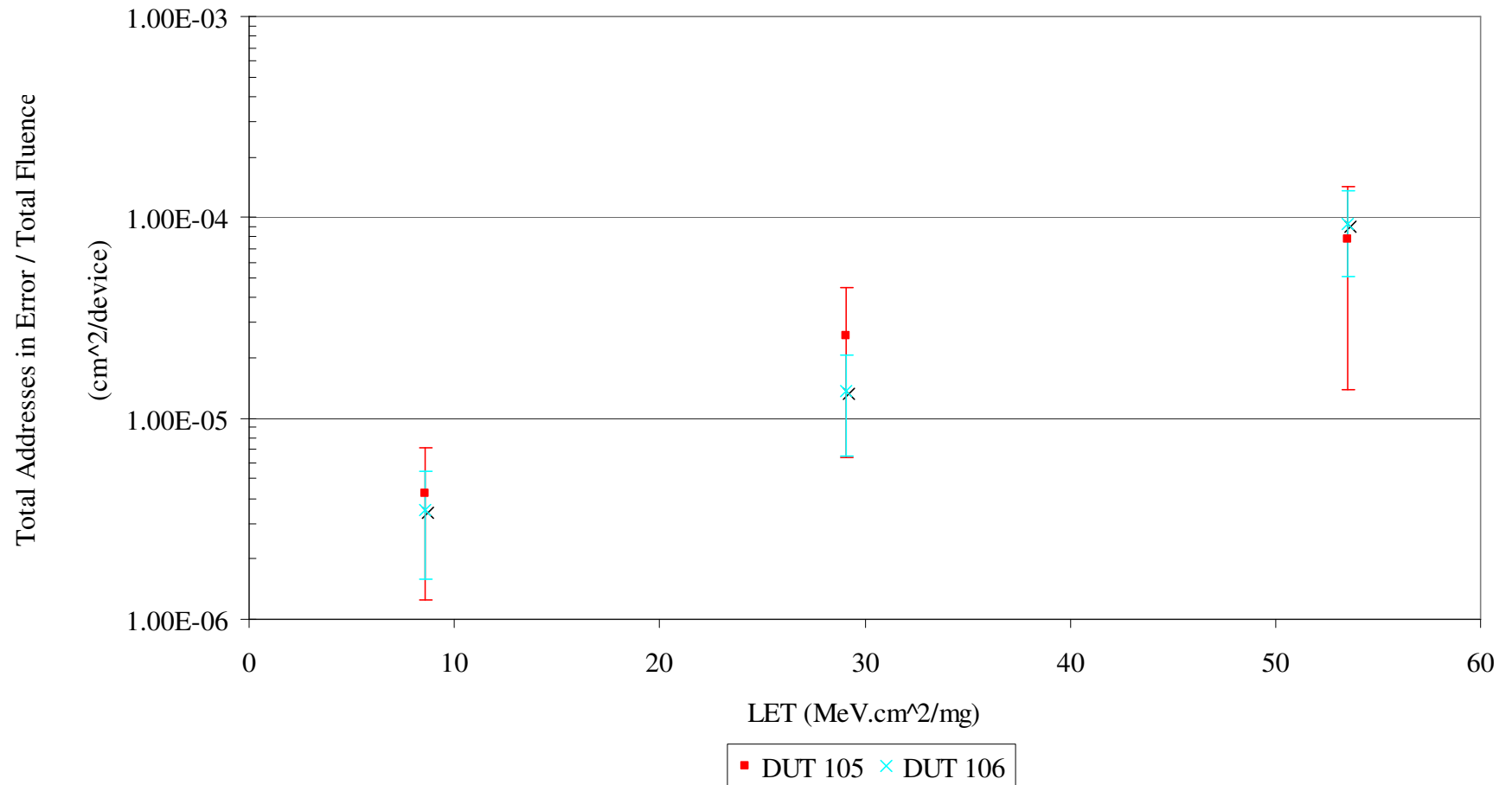


Figure 6: Dynamic Error Cross Section

Objectives Met:

1. EEPROM test pattern was controllable with a minimum requirement of an all zeros, all ones, checkerboard and reverse checkerboard patterns.
2. Testing was performed in both a static and dynamic mode. In the static test the device memory was written and verified, exposed without being exercised, and then the device was read, with errors corrected. All errors and error memory locations were recorded after static runs. The device memory was read at least three times after exposure to verify that there are no stuck bits. In the dynamic test the device memory was written and verified (to ensure the device is performing correctly prior to exposure). The device was then exposed while being exercised, recording all errors, error memory locations, and timestamp.
3. Testing was done across the Linear Energy Transfer (LET) range from threshold through 53.5 MeV-cm²/mg (Xenon at normal incidence). Sufficient ions from the list in Section III should be done to ensure a statistically significant cross section curve is developed. Normally incident ions are to be used – no testing at angles is required or desired.
4. Latch-up testing was taken into consideration for all test runs. If the supply current exceeded 300mA, i.e. latch-up occurred, the beam was powered down, as well as the supply current to the device.
5. Testing was conducted at nominal voltage (3.0 Volts).

Objectives Not Met:

1. Testing was not conducted at higher and lower voltages (3.3 Volts, 2.7 Volts).
2. Testing was not done at high temperatures.
3. Testing was not conducted with external 14V instead of the charge pump due to die connections.